

**ABSTRACT OF THE DISCLOSURE**

An evaluation circuit 16 repeats processing in which an output  $V_D$  thereof is reset, there is obtained repeatedly given times a difference between sampled output voltages  $V_O$  of a replica circuit 11R when respective times  $t_1$  and  $t_2$  have elapsed after a voltage  $V_i$  is step-inputted to the replica circuit 11R, and the differences are successively summed. A comparator circuit 20 compares a difference cumulation voltage  $V_D$  with a reference voltage  $V_S$ . A bias adjustment circuit 15 steps up the bias currents of the replica circuit 11R and an adjusted circuit 11 at every this given times if  $V_D > V_S$ , and ceases the adjustment if  $V_D < V_S$ .

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